

# Digitally Assisted Analog Circuits

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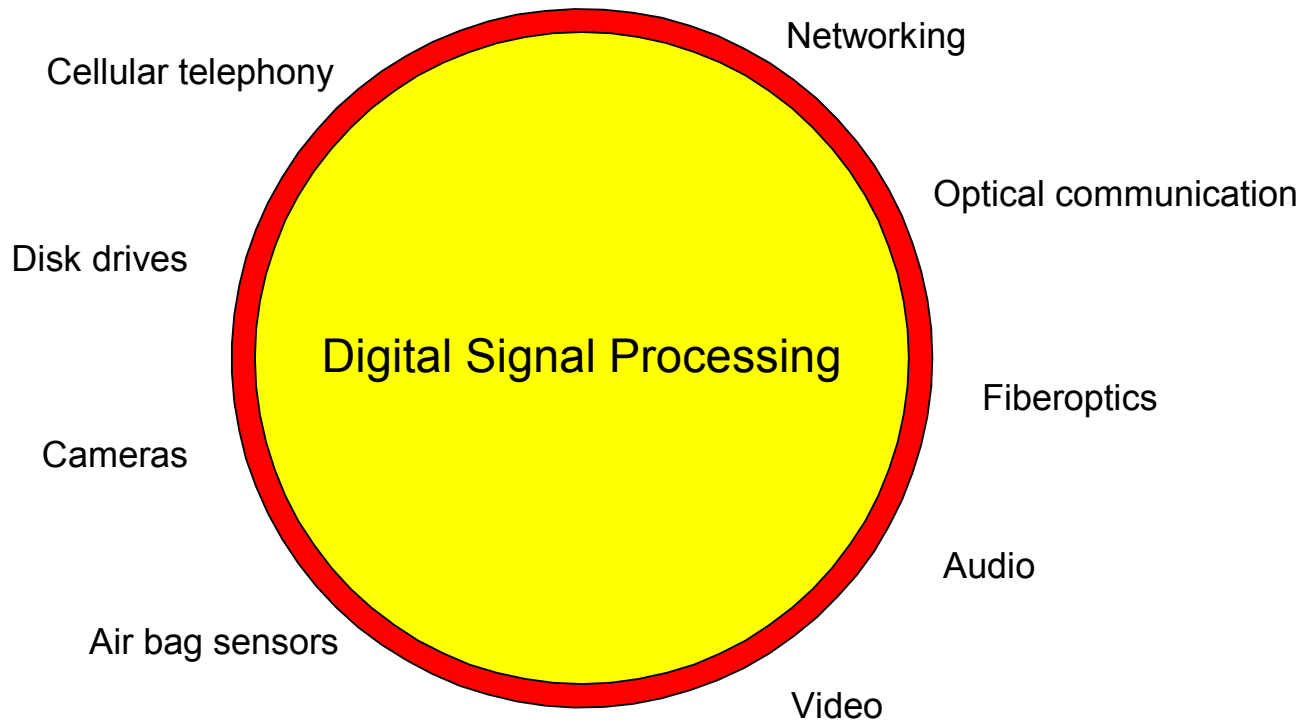


# Integrated Circuit Trends

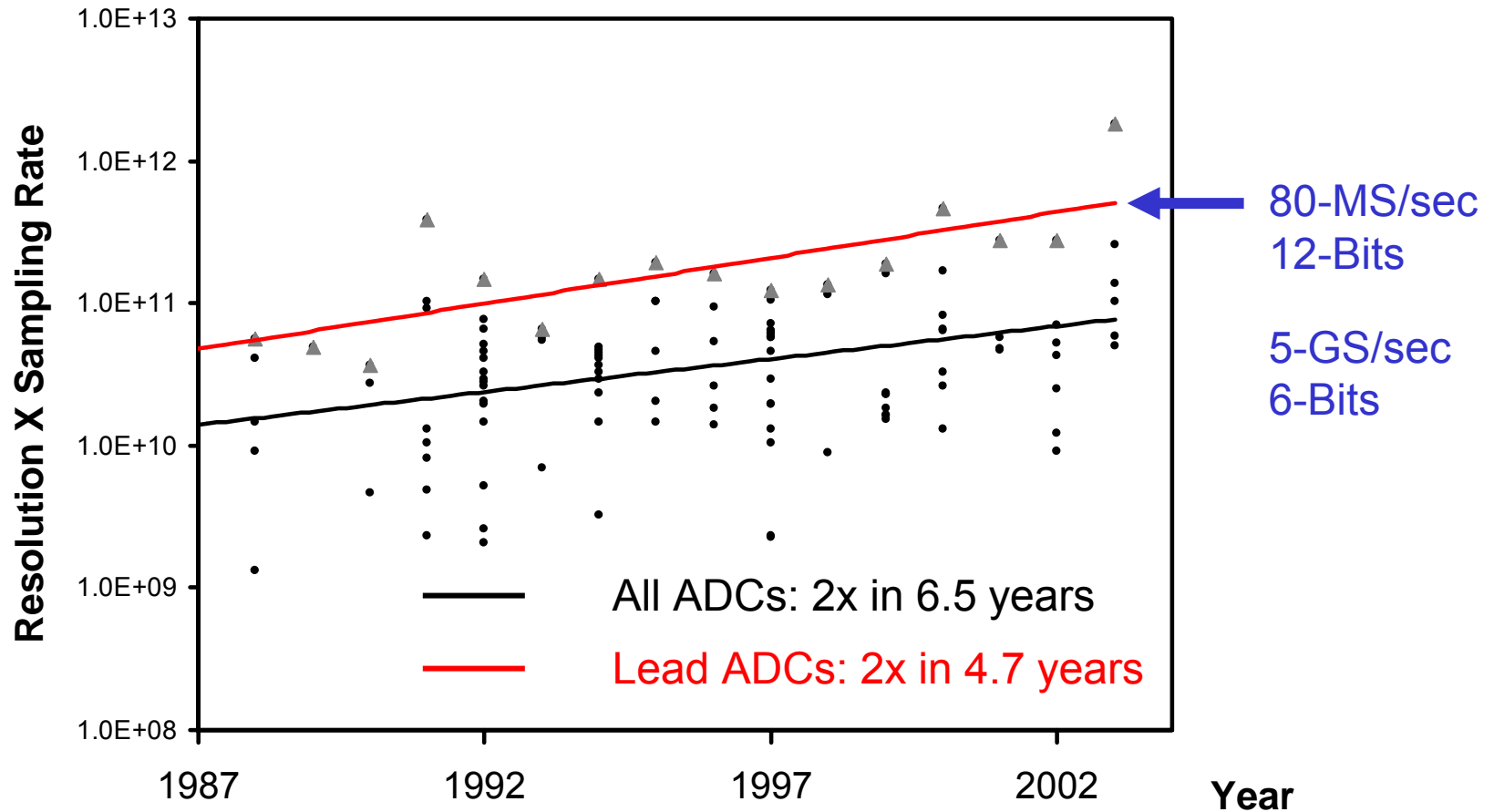
- Moore's Law
  - Transistor count doubles every 2 years
- Rapidly improving circuit performance:
  - E.g. microprocessors:
    - Clock rate doubles in 2.3 years
    - Performance doubles every 1.5 years
  - Enables new functions, e.g.
    - digital video,
    - wireless LAN, WAN, 3G, ...
- Analog circuit performance trends?
  - Present trends
  - Challenges
  - Opportunities



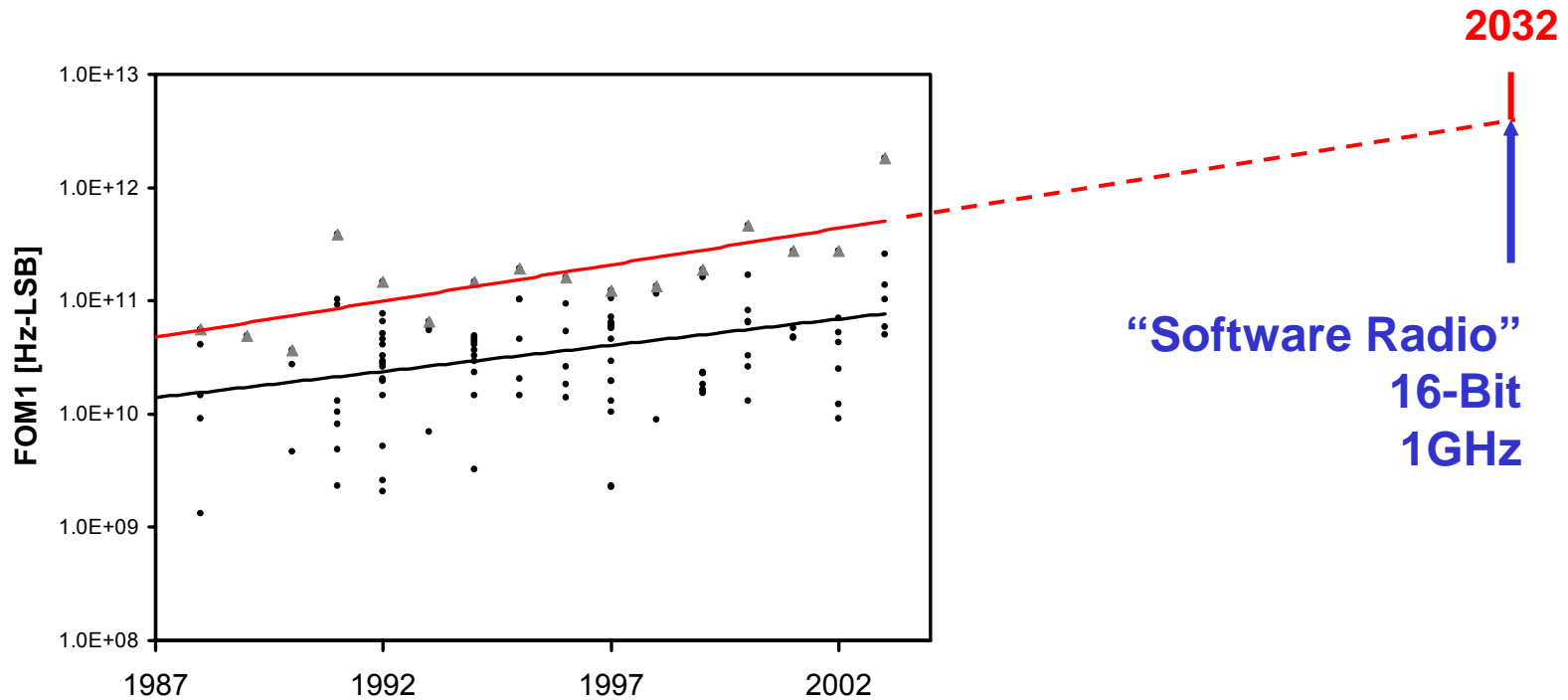
# Analog Circuit Applications



# Analog Circuit Performance (ADC)



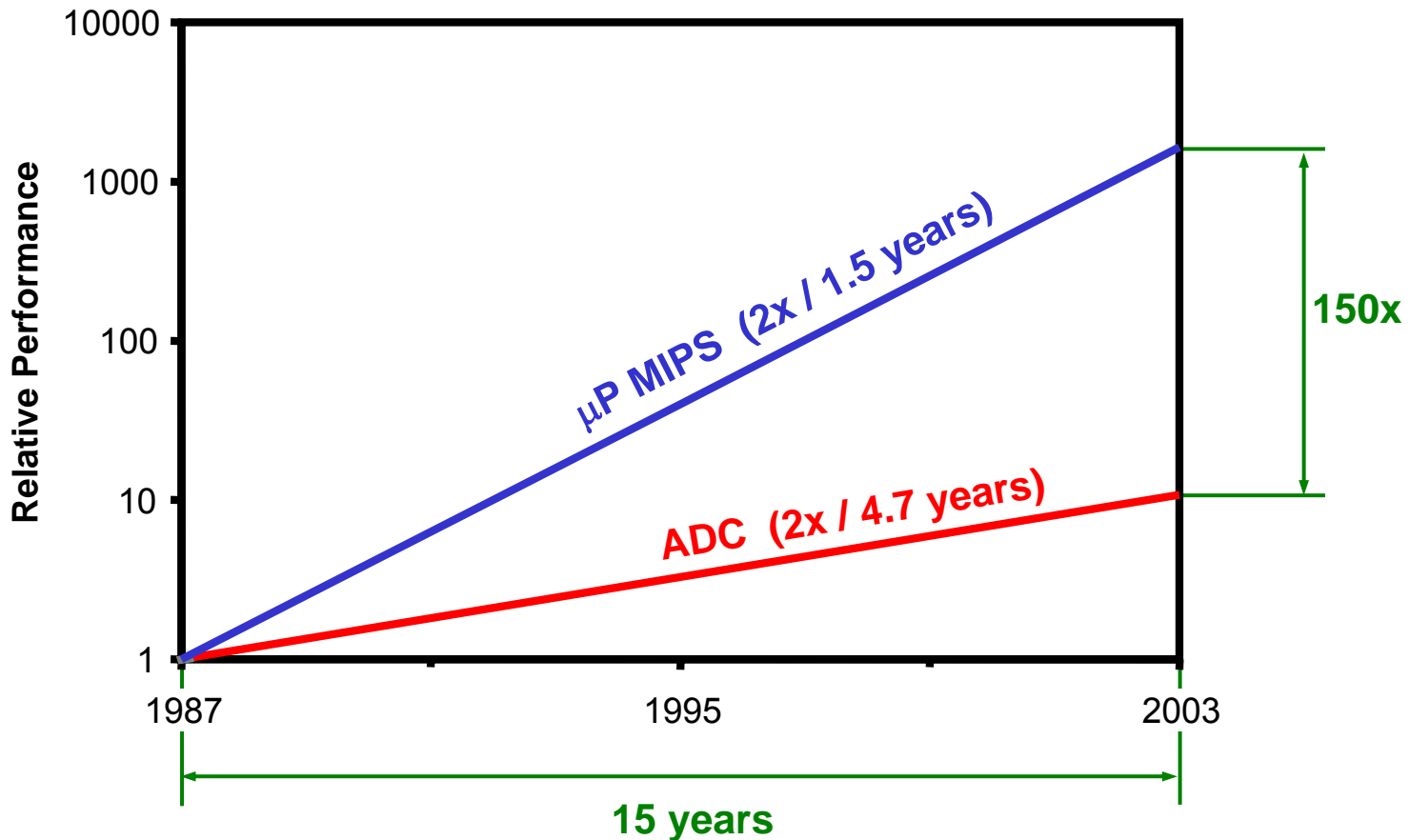
# ADC Performance Projection



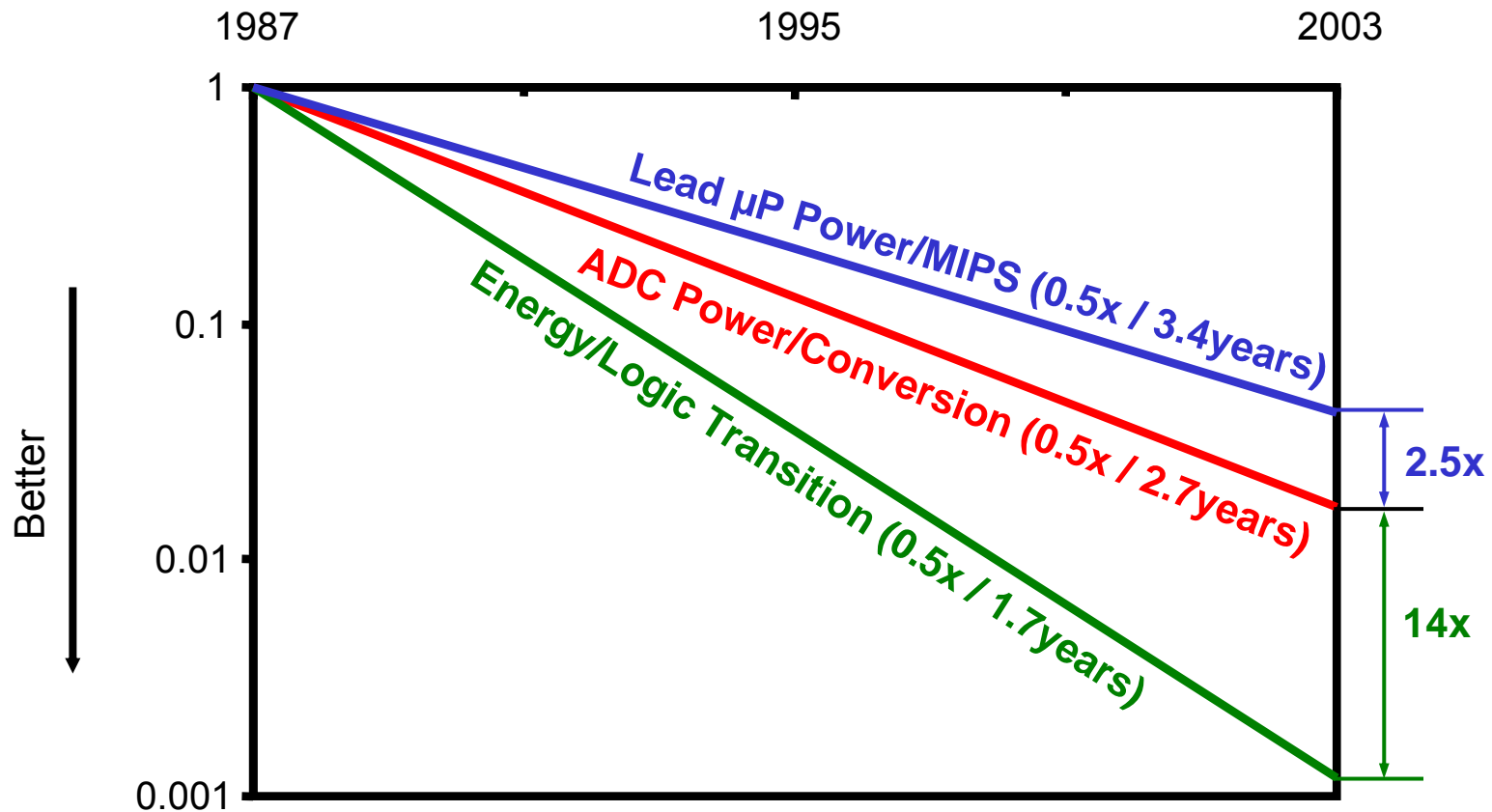
“Software Radio”  
16-Bit  
1GHz



# Analog-Digital Performance Comparison



# Analog-Digital Power Comparison



# Analog-Digital Power Comparison

## Digital

$$P_{dig} \propto CV_{DD}^2 f_{CLK}$$

C gate, wiring capacitance  
 $V_{DD}$  supply voltage  
 $f_{CLK}$  clock speed

- Reducing  $V_{DD}$  **lowers** power
- Power = f(**scaling**, C)

## Analog

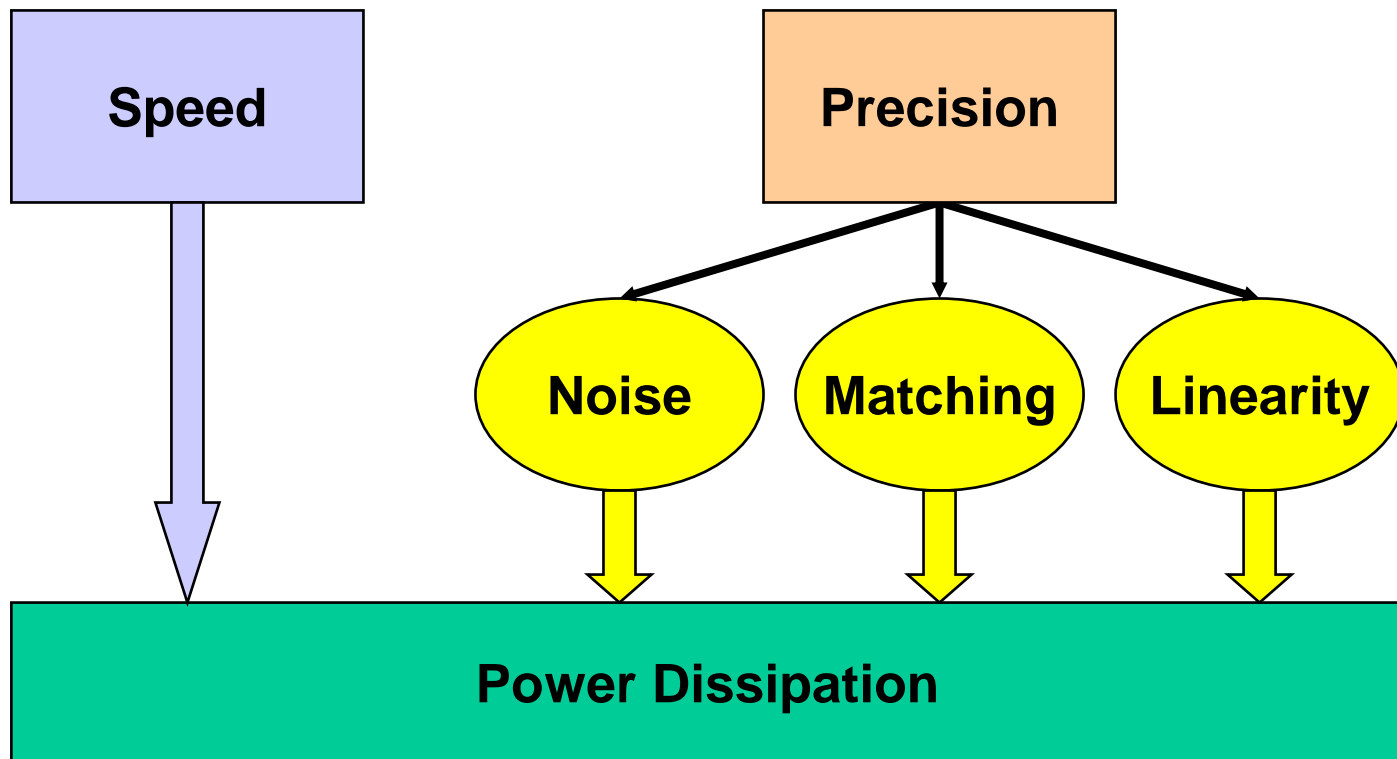
$$P_{ana} \propto \frac{2^{2B}}{V_{DD}} f_{CLK}$$

B resolution [Bits]  
 $V_{DD}$  supply voltage  
 $f_{CLK}$  clock speed

- Reducing  $V_{DD}$  **increases** power
- Power = f(**resolution**, B)

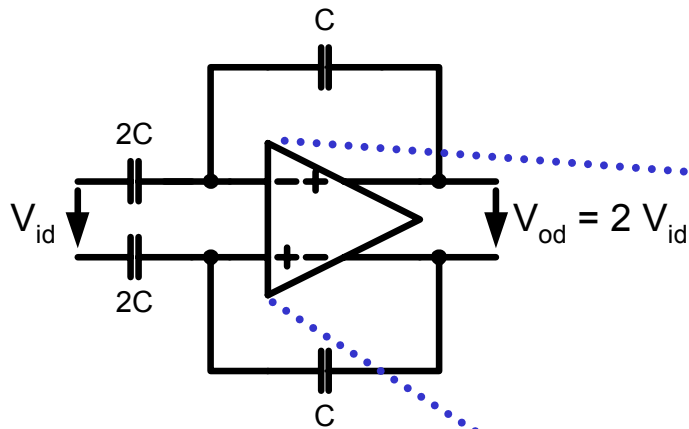


# Analog Circuit Challenges

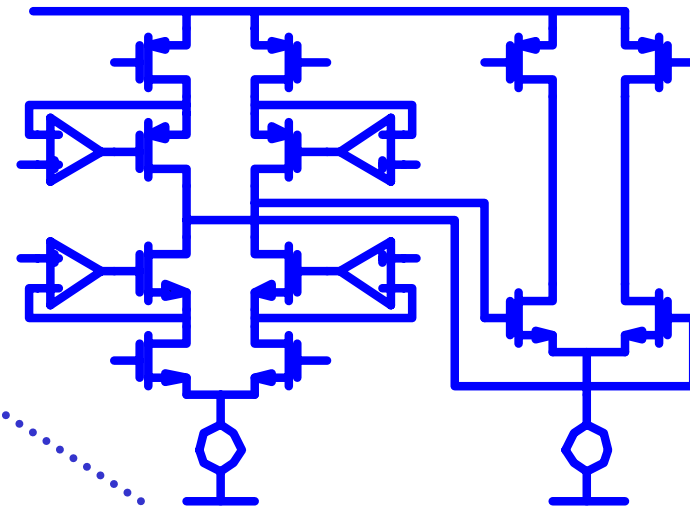


# Analog Precision Techniques

## Feedback

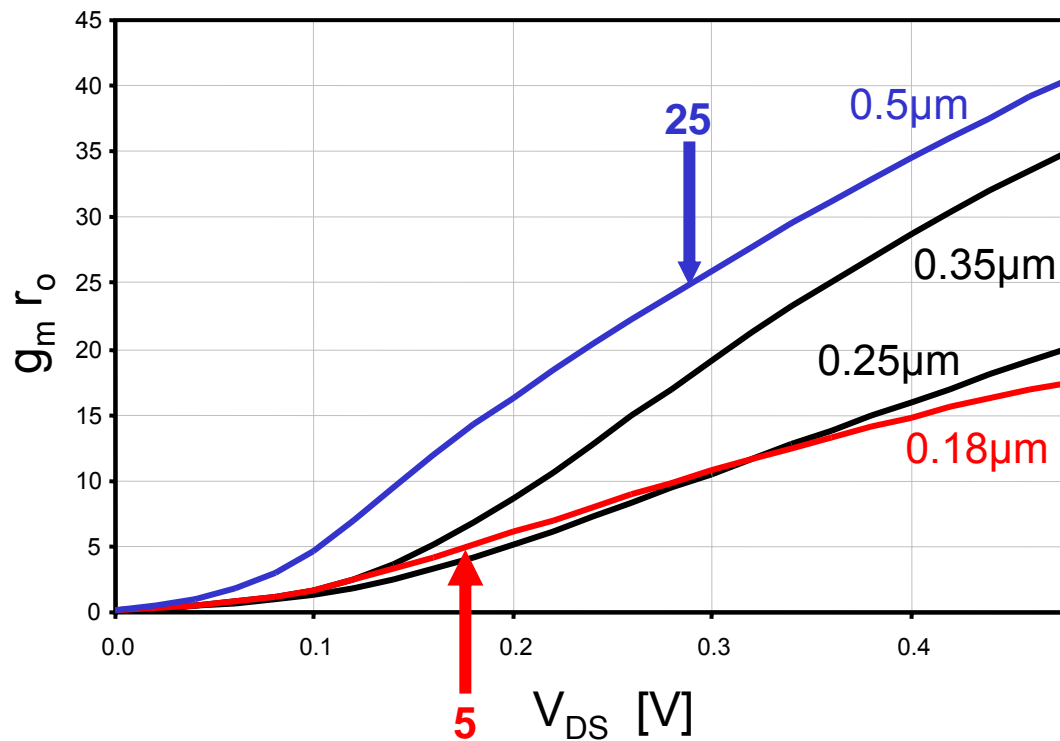


Gain = 2



Gain = 100,000

# Intrinsic Transistor Gain



Channel length  $L \downarrow$   
Gain  $\downarrow$

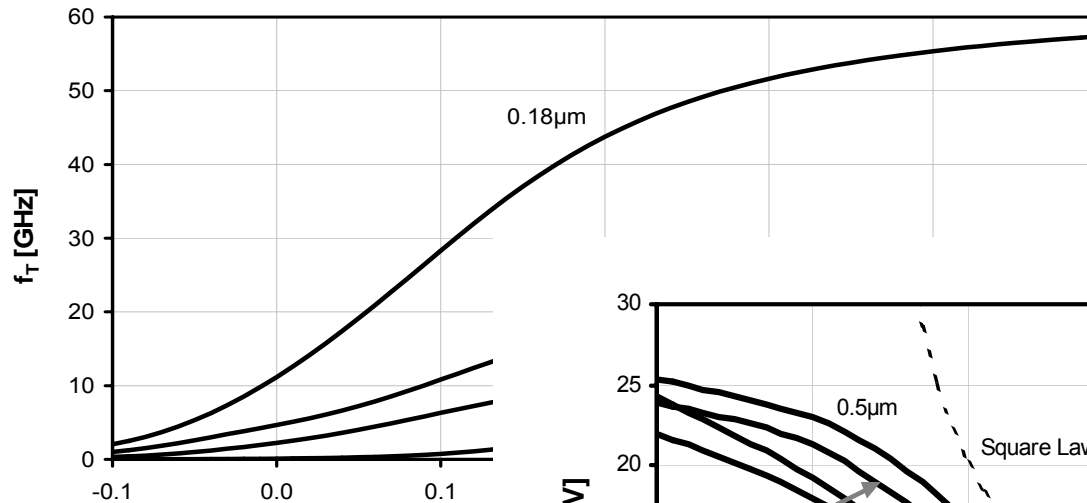
Scaling "hurts"

# Consequences ...

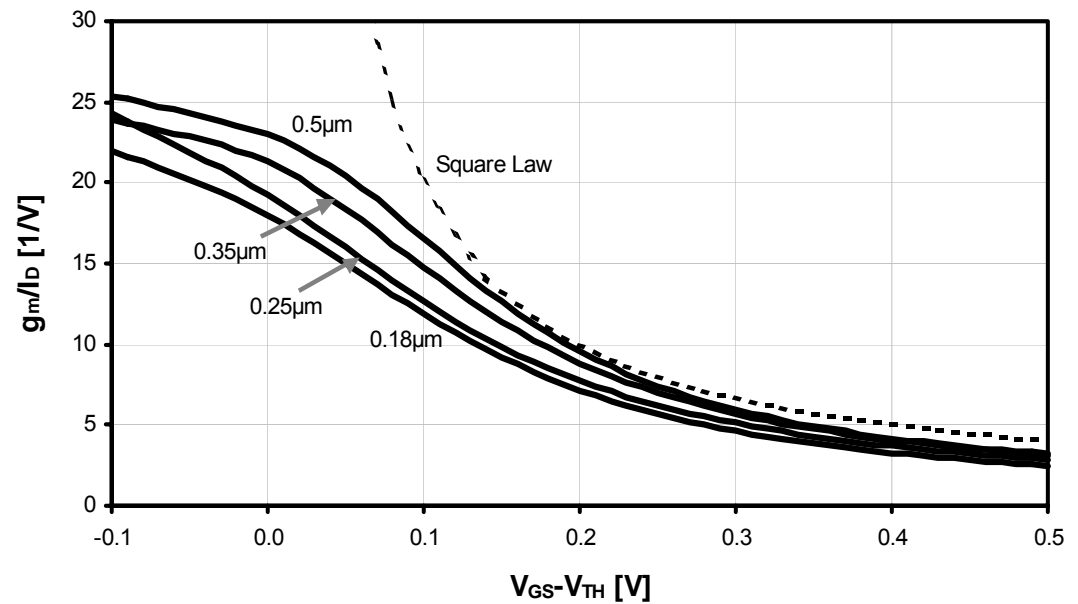
- [Annema, TCAS99]:
  - “The overall effect is that power consumption decreases with newer CMOS processes down to about 0.25 or 0.35  $\mu\text{m}$ .”
  - “The trend that power consumption increases with decreasing supply voltage was shown to be fundamental ...”
- [Annema, PlanetAnalog, 2004, <http://www.planetanalog.com/printableArticle.ihtml?articleID=17701355>]
  - “In conclusion, analog circuits can benefit from technology scaling if the supply voltages are not scaled down, unlike in their digital counterparts.”
- [Bult, ISSCC99]:
  - “Power dissipation generally increases if a circuit operates under reduced signal swing conditions to maintain performance.”
- **Scaling has no benefits?**

# Scaling Benefits

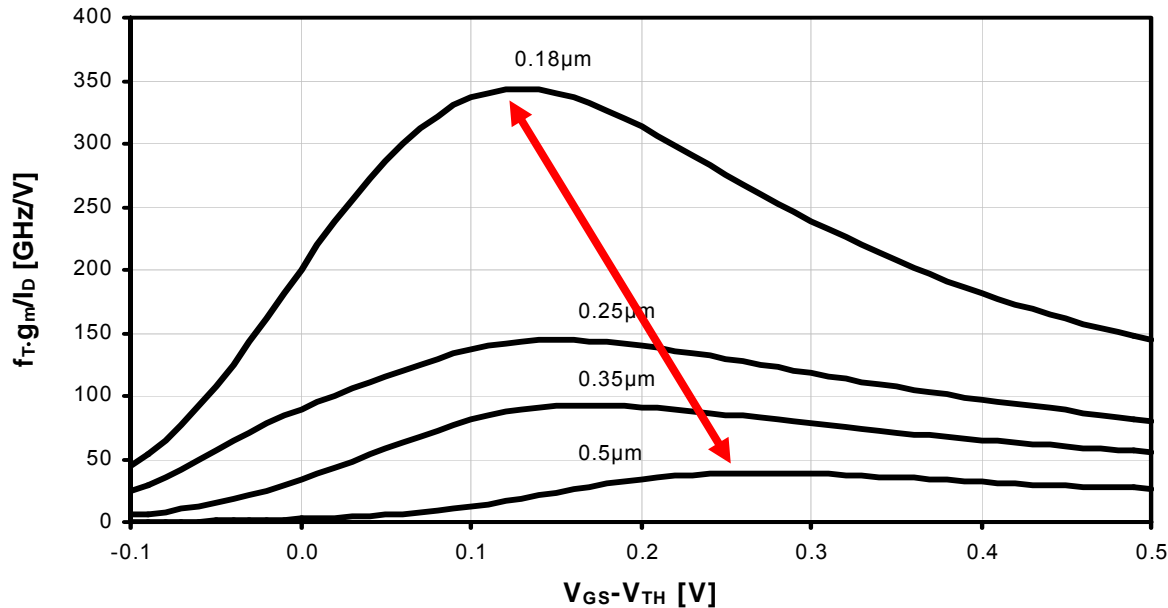
Intrinsic speed ( $f_T$ )



Efficiency  $g_m/I_D$



# Transistor Performance



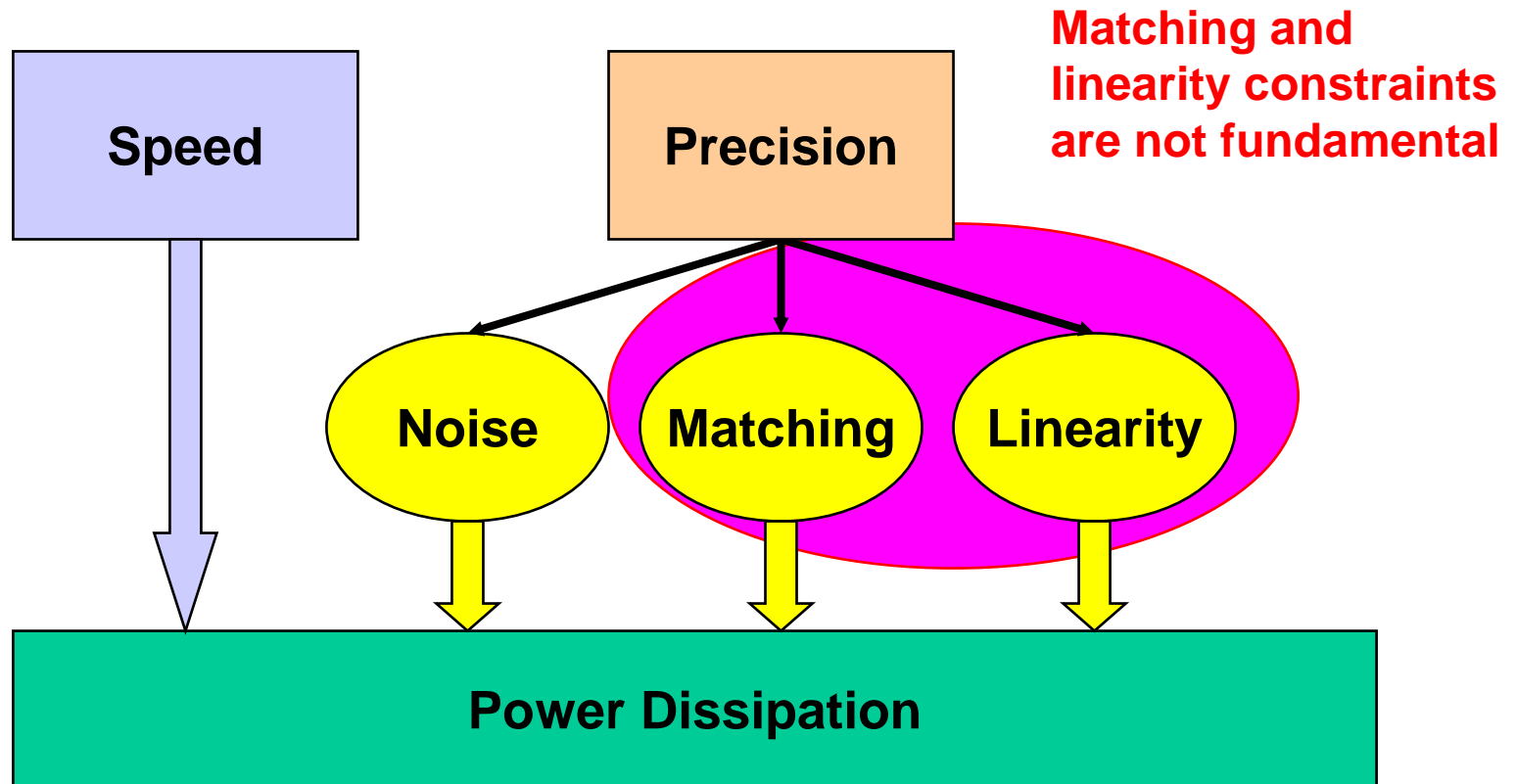
**Scaled transistor:  
Significantly better performance at lower voltage**

# Technology Scaling

- Device performance improves
  - Speed ( $f_T$ )
  - Power efficiency ( $g_m / I_D$ )
- Digital circuits
  - Capitalize on improved devices
  - Clock rate doubles every 2.3 years
  - Performance (MIPS, SPECint) doubles every 1.5 years
- Analog circuits
  - Low supply, intrinsic device gain negatively impacts precision
  - Relative performance increasingly lags that of digital circuits
  - Performance doubles in 5 years
  - Over 15 years, analog/digital performance gap is  $\sim 150x$
- Is this also a “law”

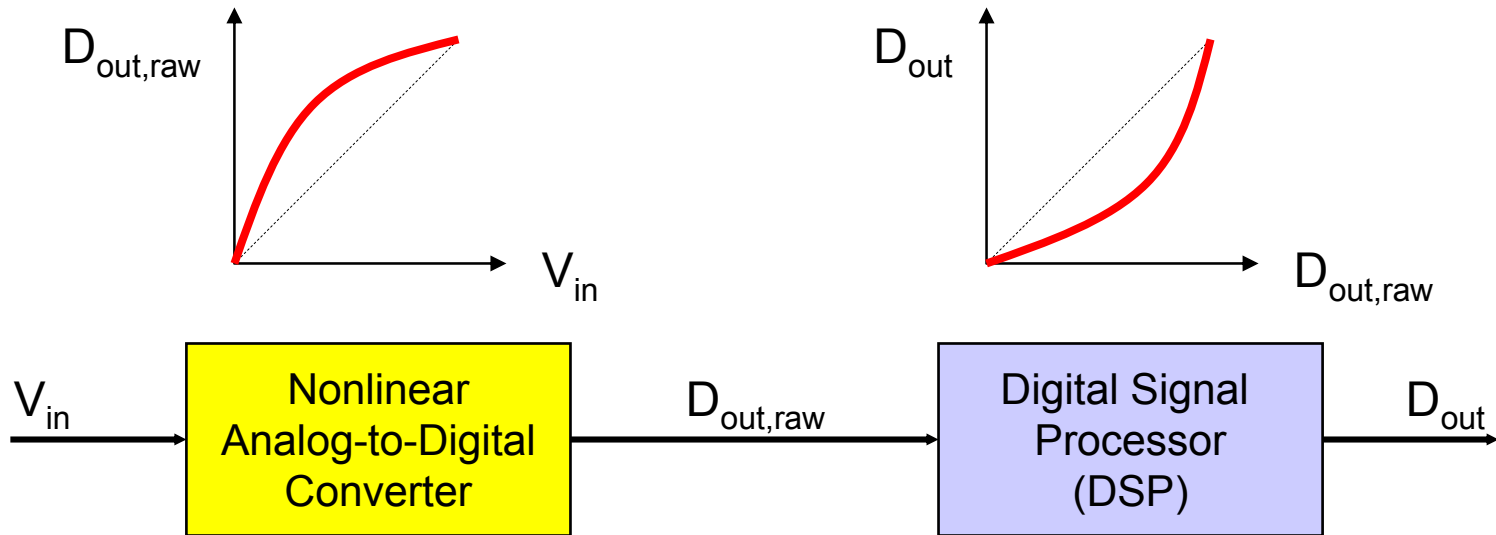


# Analog Circuit Challenges





# Analog Circuit Nonlinearity

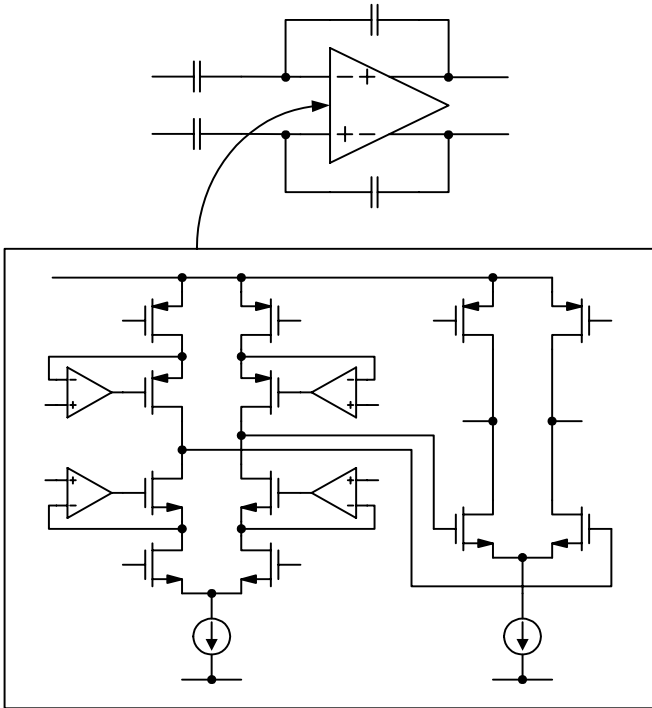


$$D_{out,raw} = f(V_{in})$$

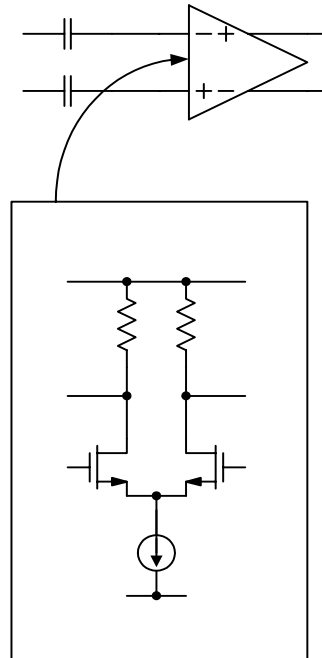
$$\begin{aligned} D_{out} &= f^{-1}(D_{out,raw}) \\ &= f^{-1}(f(V_{in})) \\ &= V_{in} \end{aligned}$$

# Open-Loop Amplification

Precision Amplifier

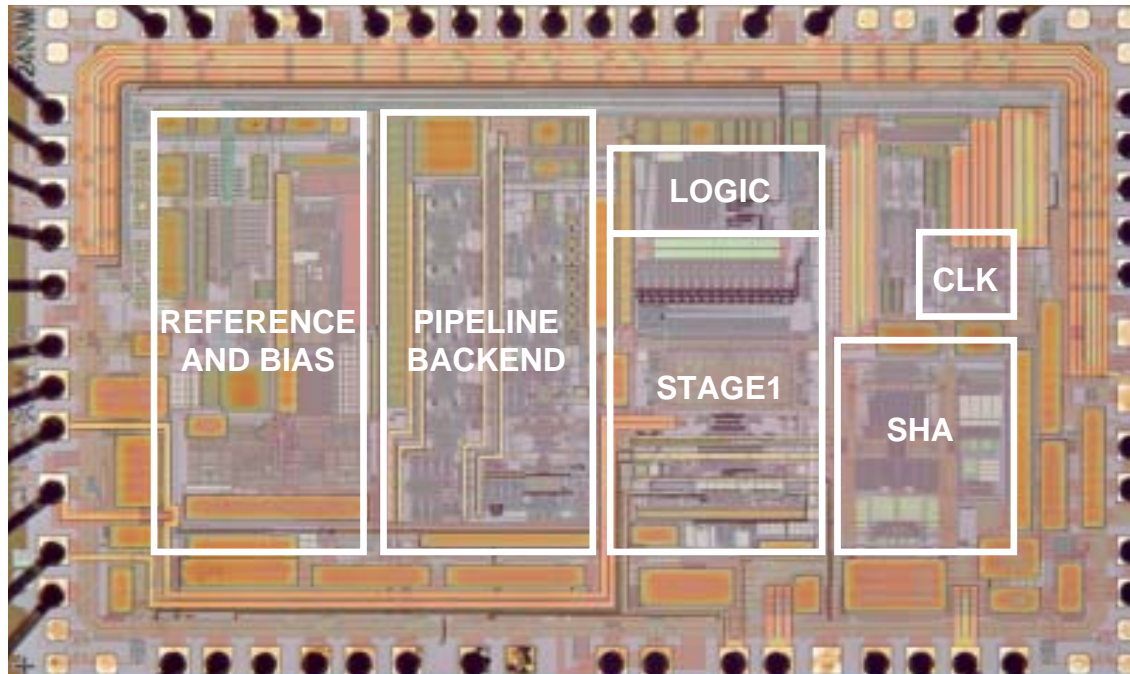


“Open loop”



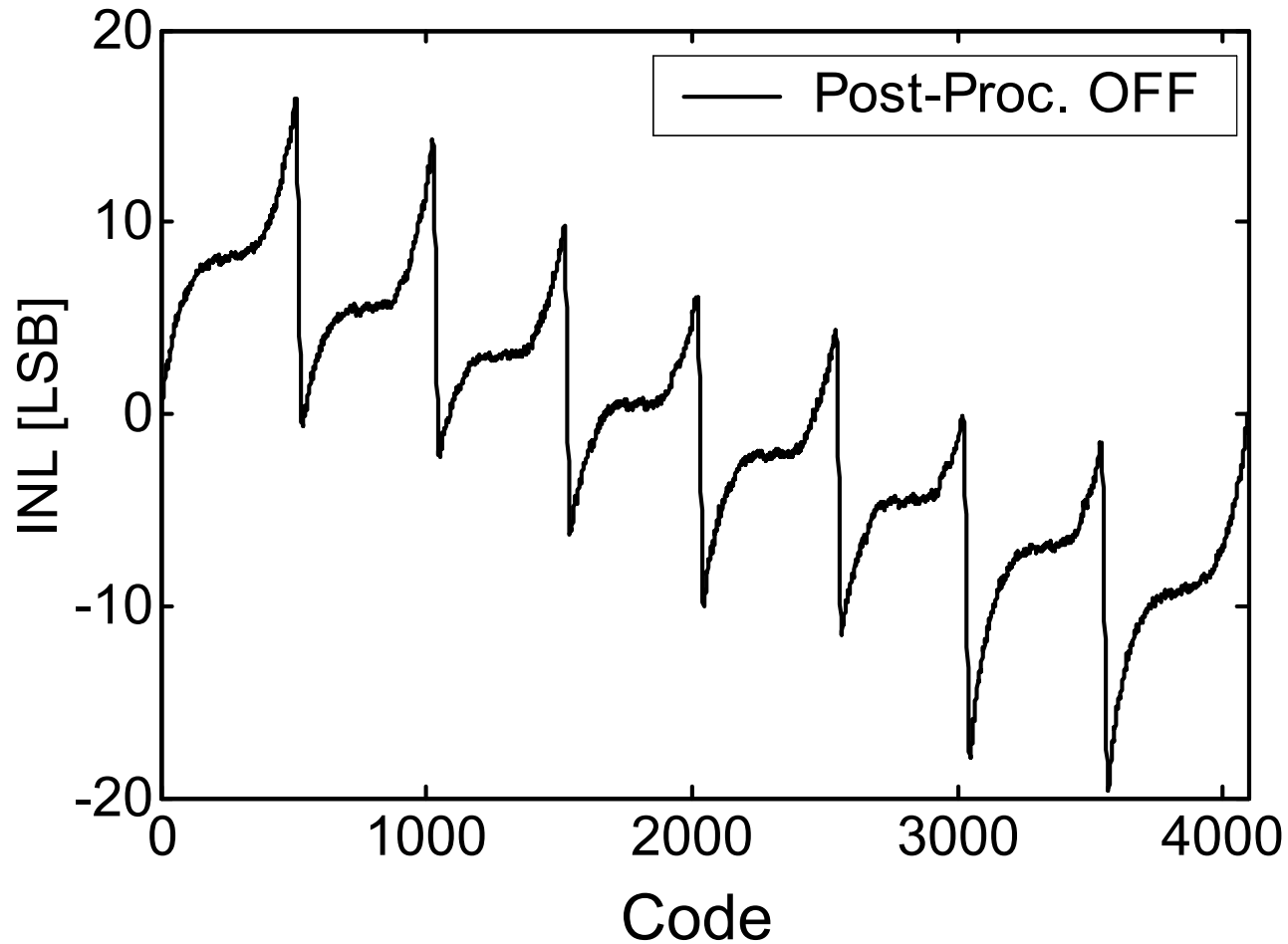
- + Faster
- + Lower Power
- + Lower Noise
- + Increased Signal Range
- Nonlinear
  - Use DSP to linearize!
- ✘ **Practical?**

# Experimental Verification

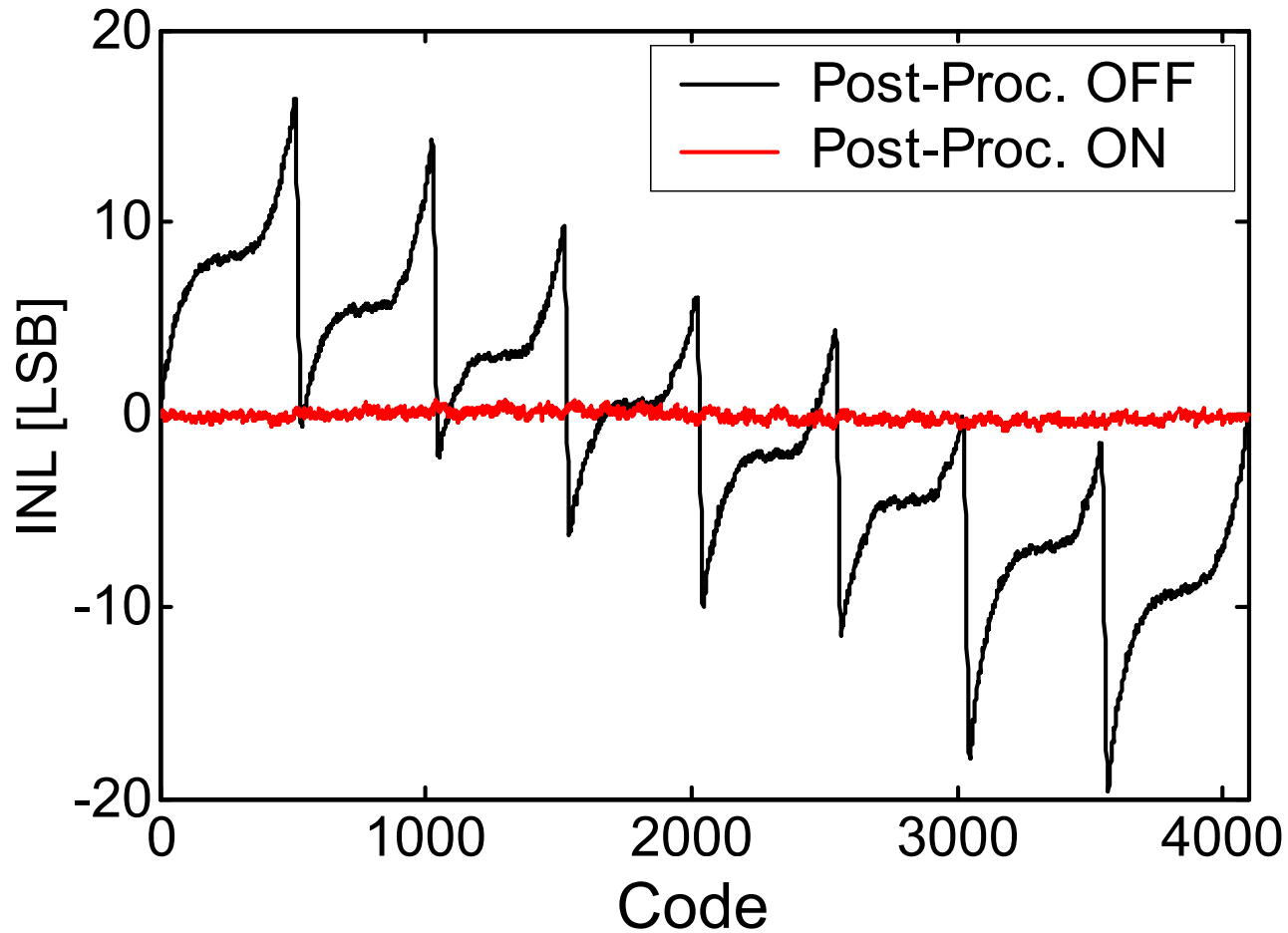


- 12bit, 75MHz, 0.35 $\mu$ m, post-processor off chip
- Based on commercial part (Analog Devices AD9235)

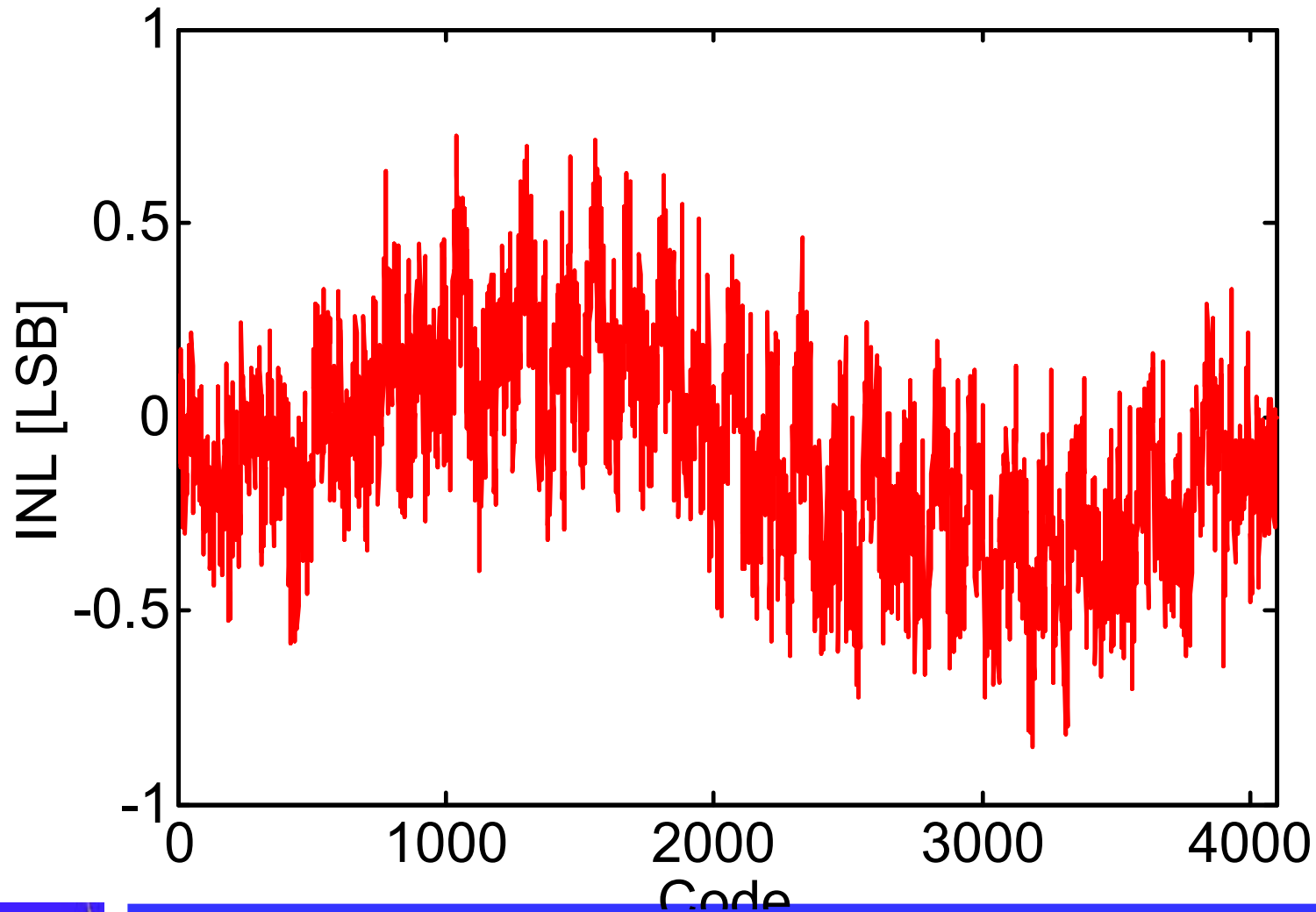
# Measured INL



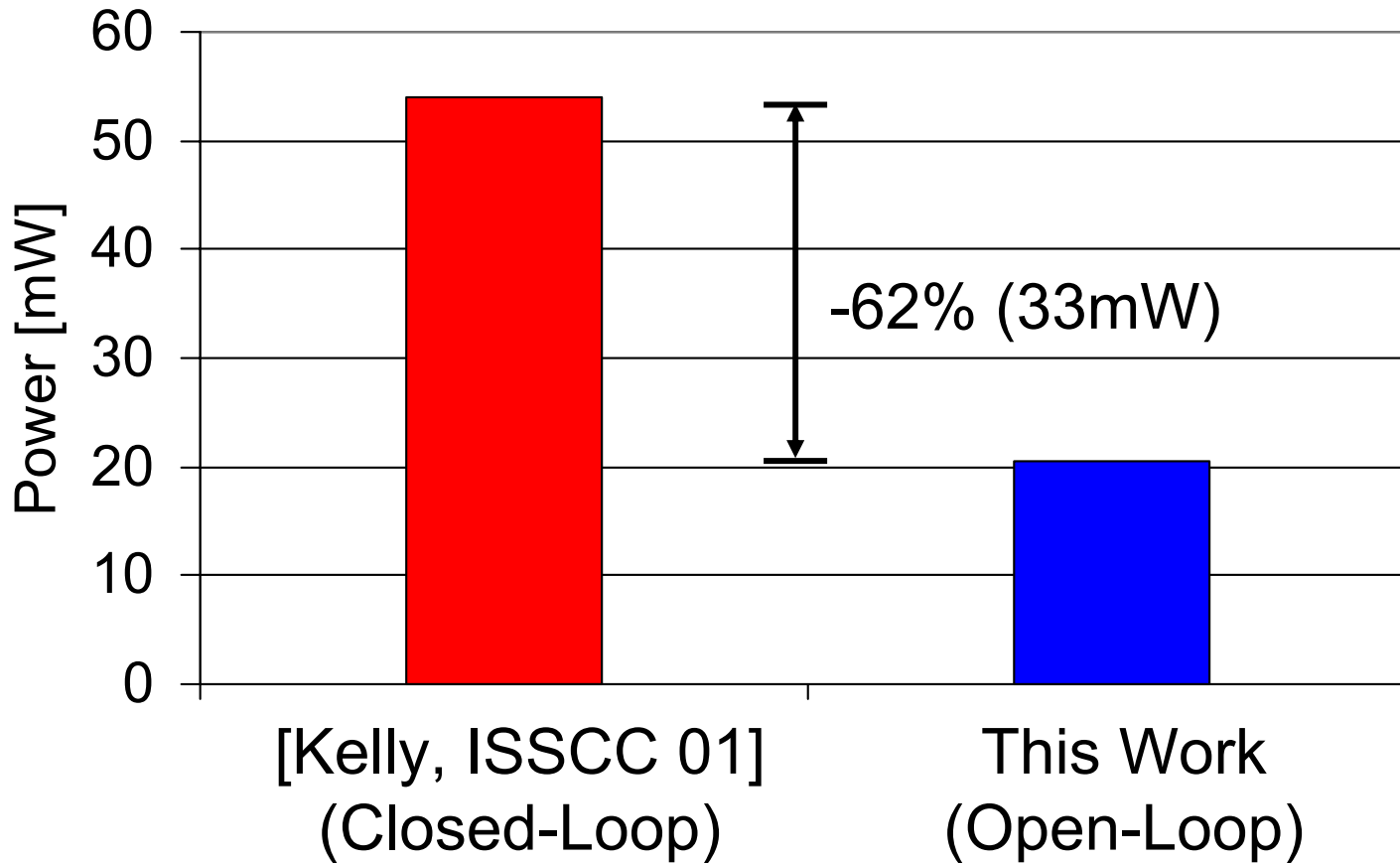
# Measured INL



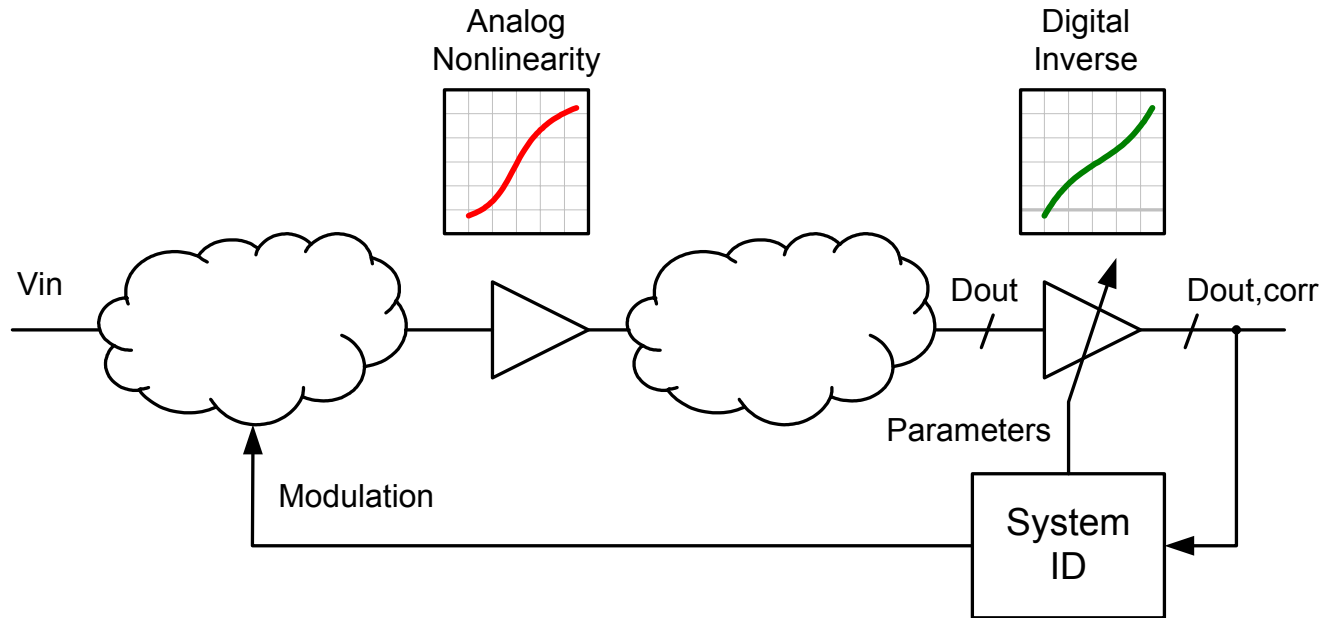
# INL Zoom (Post-Proc. ON)



# Stage1 Amplifier Power



# Digital Nonlinearity Correction



- System ID determines optimum post distortion
- Background operation tracks variations over time without interrupting normal circuit operation

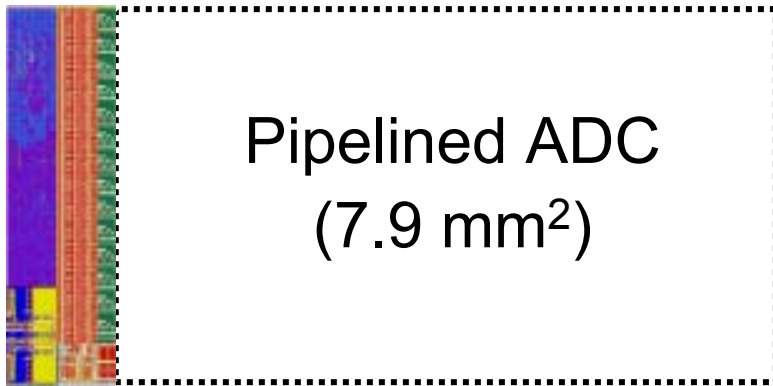


# Digital Post-Processor

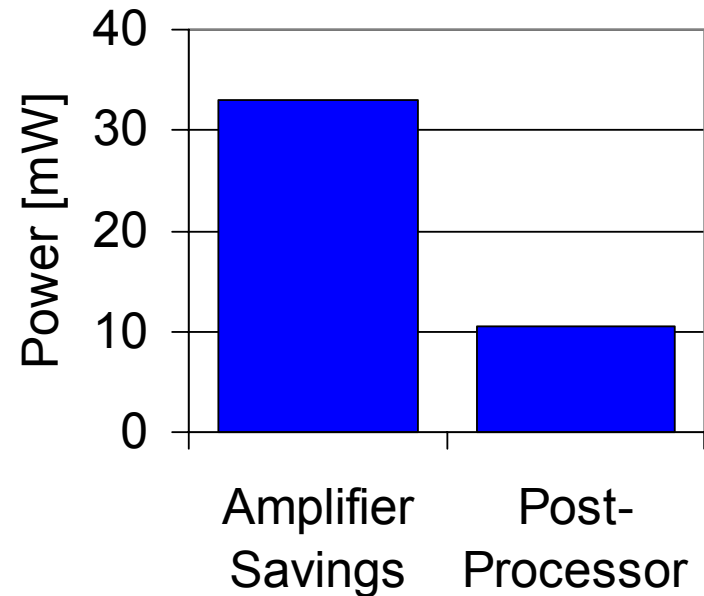
- 8400 Gates, 64 bytes RAM, 64kBit ROM
- Implementation in 0.35 $\mu$ m technology

Area=1.4mm<sup>2</sup> (18%)

Power=10.5mW (3.6%)

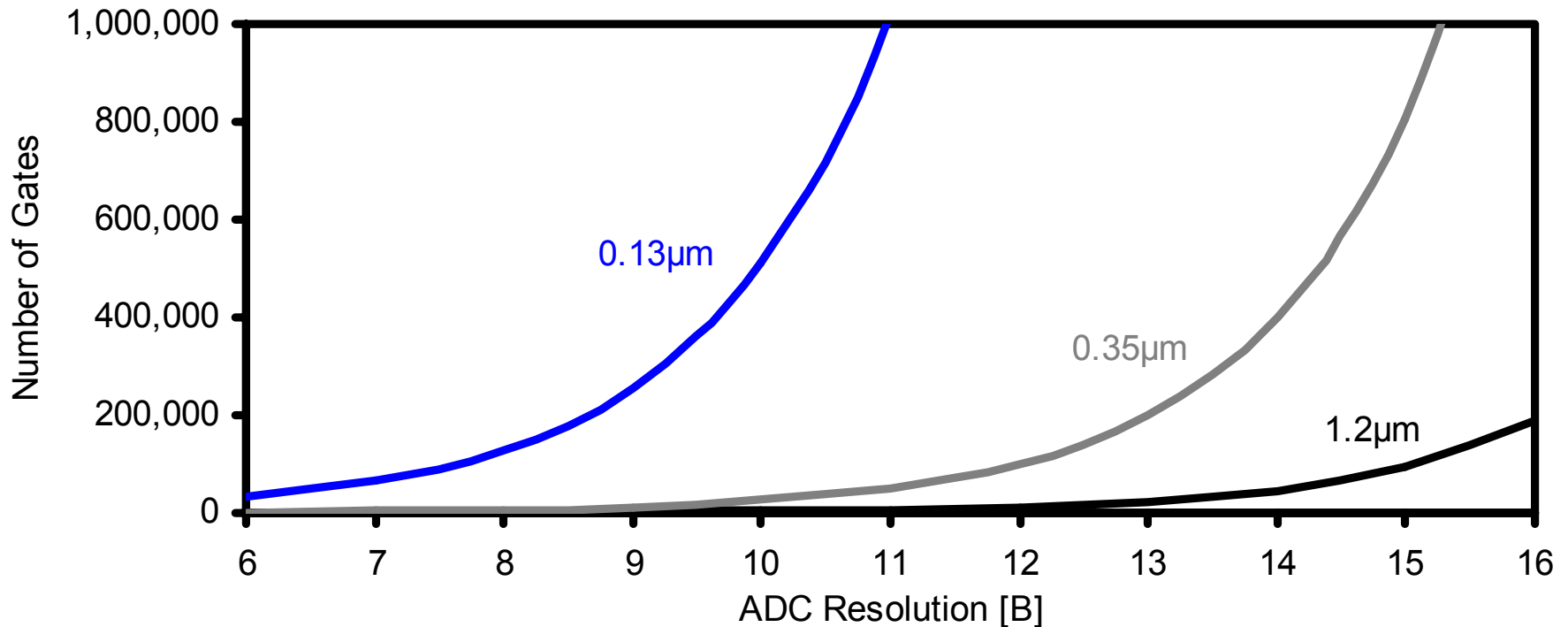


Post-Processor

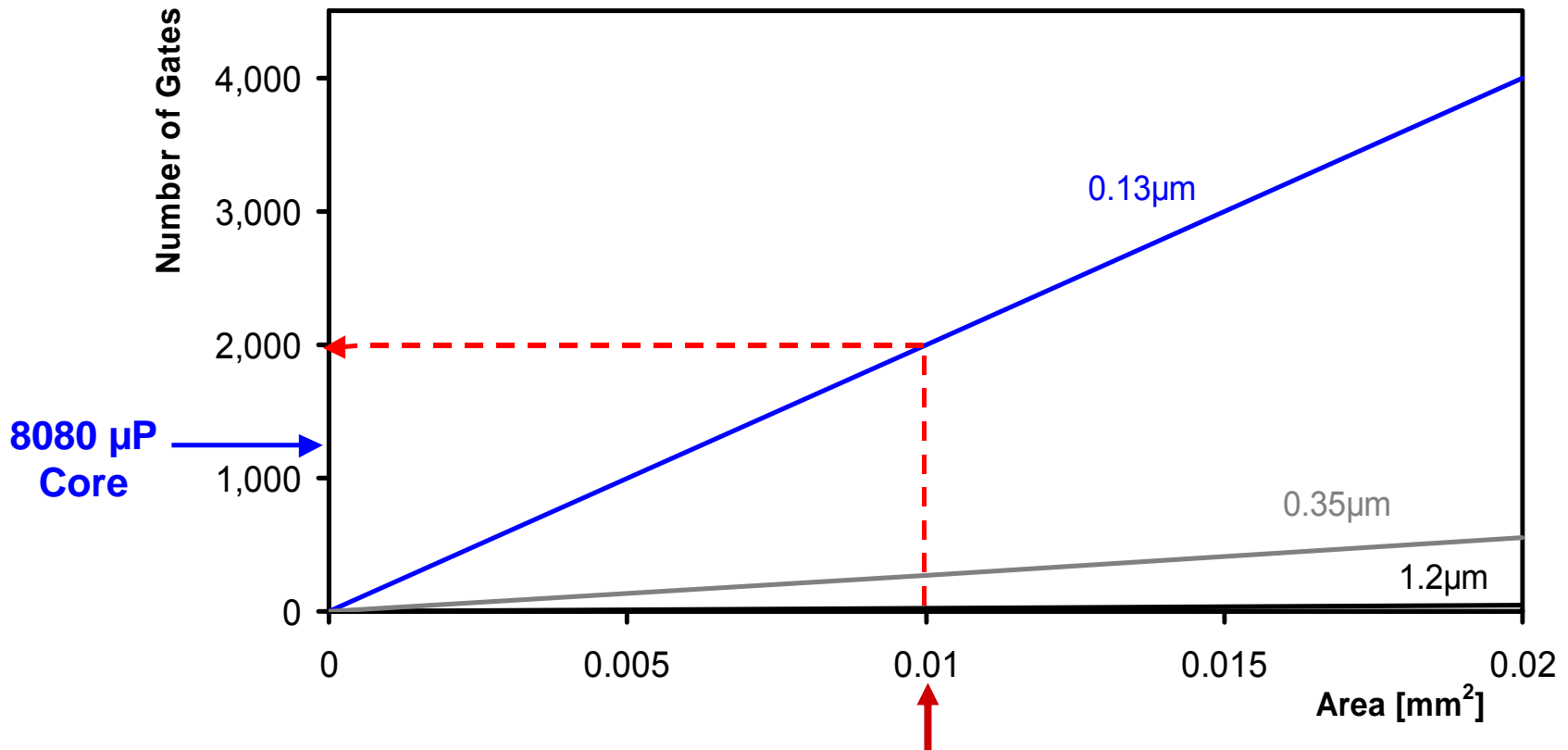


# Analog / Digital Power Comparison

"Number of logic gates with same energy consumption as a state-of-the-art B-bit ADC"



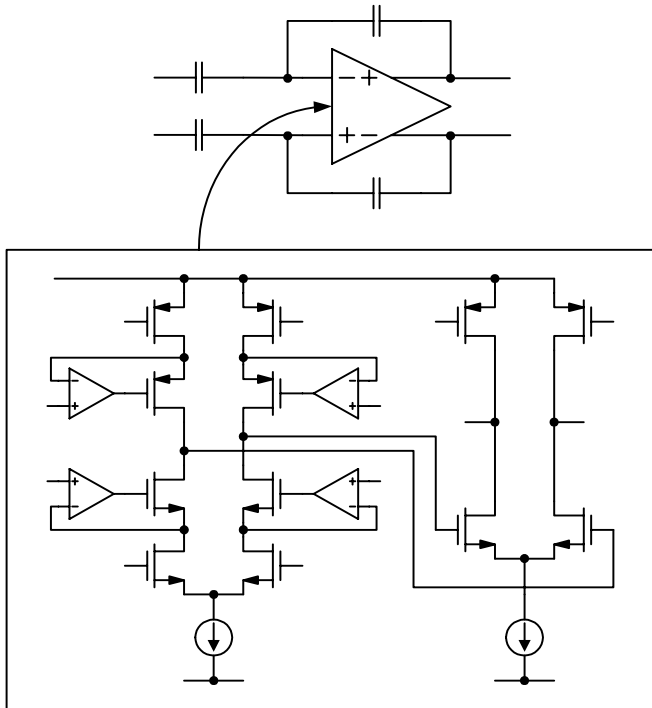
# Analog / Digital Area Comparison



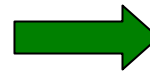
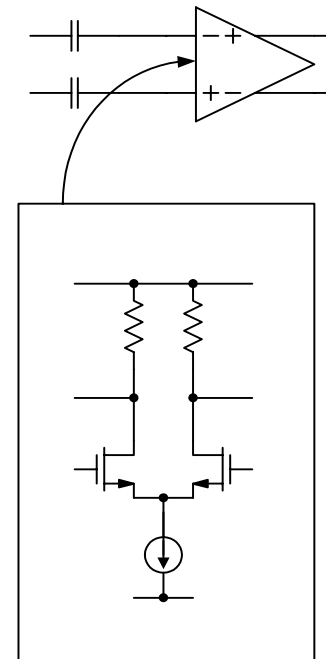
**Area of a 10pF integrated (linear) capacitor**

# Circuit Issues

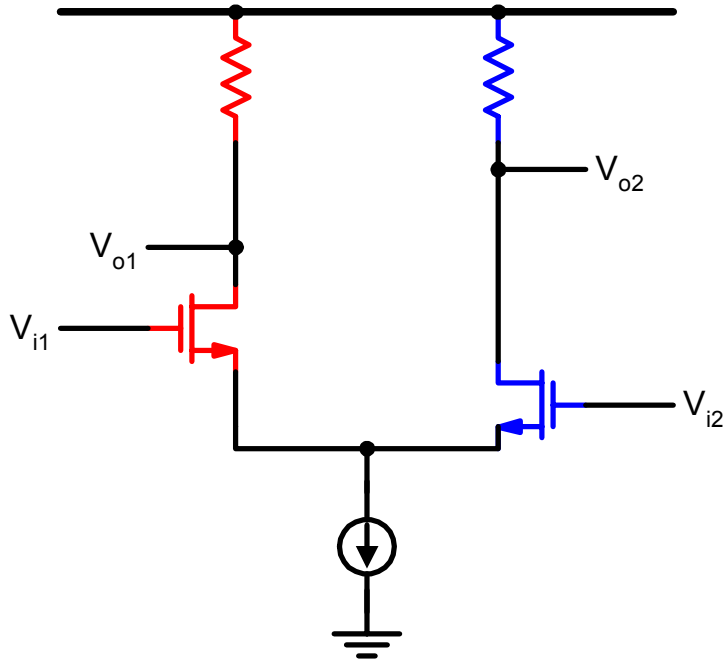
Precision Amplifier



“Open loop”

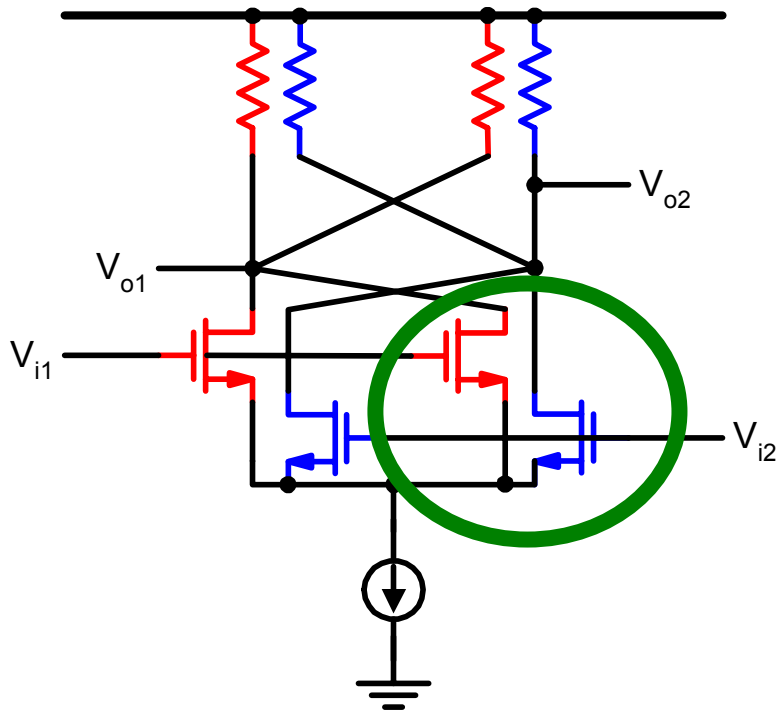


# Self-Heating



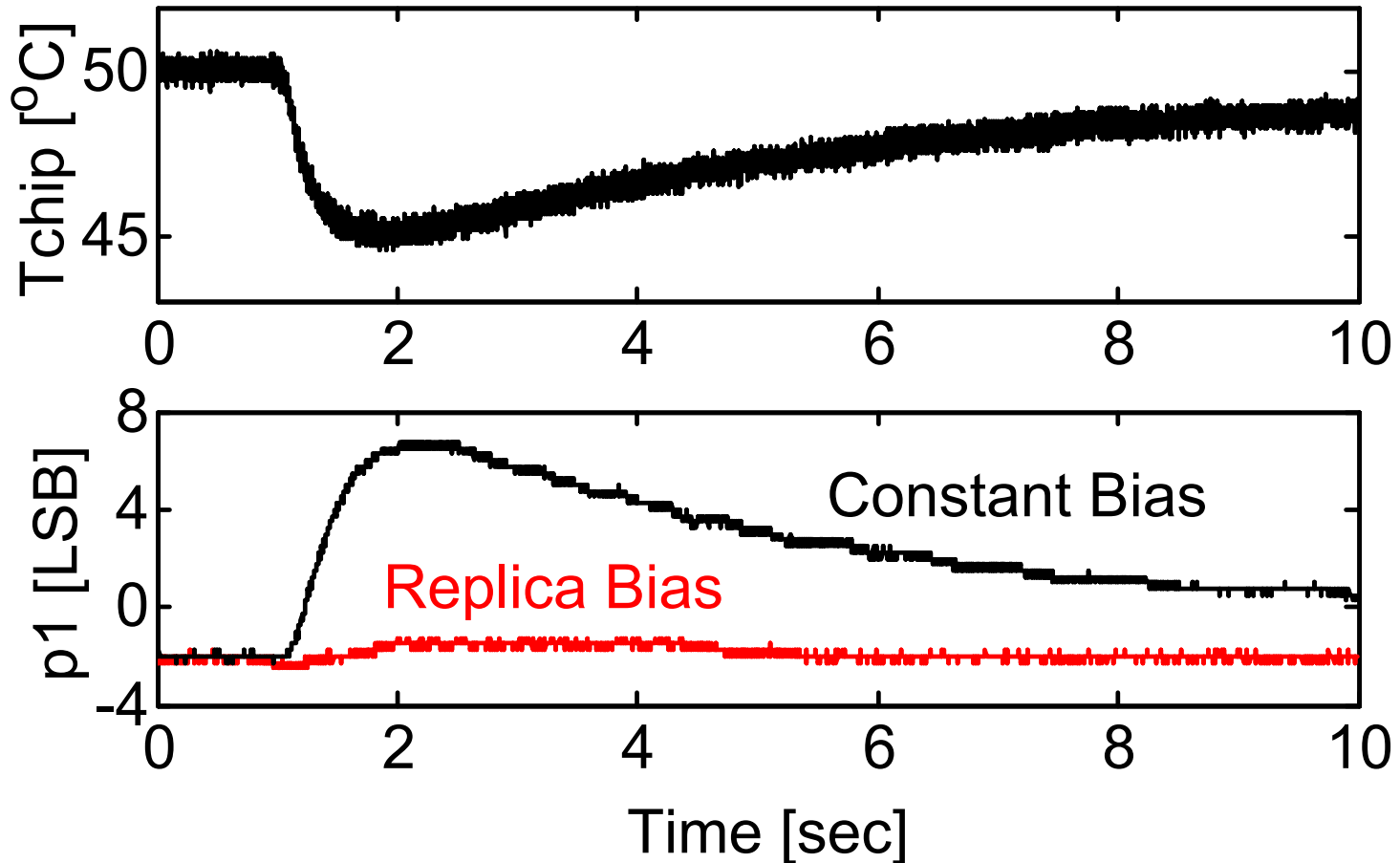
- Signal dependent current
- Signal dependent device temperature & characteristics
- Background calibration too slow to track changes

# Device Interleaving



**Interleaved layout**  
→ uniform temperature distribution

# Reduced Temperature Sensitivity



# Conclusion

- Technology scaling trends are only conditionally beneficial for analog circuit performance
- Analog circuit improvements lag progress of digital functions
- Digitally assisted analog circuits offload accuracy constraints to digital processor
- Benefits:
  - Improved analog circuit performance
  - Profit from future technology scaling



# Acknowledgements

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# Book



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